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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,900	02/26/2002	Vipul Anil Desai	CR00249M	2757

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EXAMINER	
STEELMAN, MARY J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,900	DESAI ET AL.	
	Examiner	Art Unit	
	Mary J. Steelman	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/26/02,5/23/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/26/02,5/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are pending.

Information Disclosure Statement

2. IDS submitted 2/26/2002 and 5/23/2003 has been considered.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: The oath references "Title 37, Code of Federal Regulations, Section 1.56(a)", should be --...1.56...--. Remove the '(a)'

See MPEP Chapter 2000 - Duty of Disclosure, 37 CFR 1.56.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 6,513,146 B1 to Yonezawa et al.

Per claim 13:

A method of estimating a relative power consumption of a software algorithm, comprising:

-establishing a relative energy database listing a plurality of micro-operations, each micro-operation having an associated relative energy value;

(Yoneczawa: Col. 25, lines 65-67, "FIGs. 27(a) through 27(c) are tables (relative energy database) for respectively showing a power analysis result, the power information an a power analysis result obtained after changing the program..." Micro operations such as set, add, mul, mov, ret, as shown in the drawings, are related to power consumption.)

-determining the relative power consumption of the software algorithm incorporating one or more or the micro-operations based on the relative energy values of the incorporated micro-operations.

(Yoneczawa: See Fig. 27(a) shows the power consumption of the software algorithm before optimizing. Fig. 27(c) shows the power consumption of the software algorithm after a shift operation has replaced a mul operation.)

Per claim 14:

-executing the software algorithm on a simulator;

(Yoneczawa: Col. 23, lines 9-15, "...instruction set simulator (ISS) is a simulator for conducting simulation in accordance with instructions of a program...the instruction set simulator is

aggregate of software having functions to conduct the same operations as the microcomputer", col. 24, lines 48-49, "The power analysis system of this example functions as an instruction set simulator.")

-computing a sum of the relative energy values of the micro-operations contained in the executed software algorithm.

(Yonezawa: Col. 2, lines 54-57, "...calculating a sum of the power consumption of all of the functions as total power consumption by estimating the power consumption of each function..." See FIGs. 27(a)-27(c). Analysis / sum of relative energy values of the micro-operations.)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 4,574,348 to Scallon.

Per claim 1:

A method of forming a compound Single Instruction/Multiple Data instruction, said method comprising:

(Scallon: col. 20, line 22-col. 22, line 9, "...method...")

-selecting at least two Single Instruction/Multiple Data operations of a reduced instruction set computing type;

(Scallon: Col. 2, lines 57-63, "The program has a plurality of complex instructions...The plurality of ALUs are operative to process data in accordance with the complex instructions wherein each ALU is operative in response to a predetermined one of the segments of the complex instructions..." See FIG. 3 Col. 4, lines 43-60, "an instruction processing unit generates the sequential instruction stream, but each generated instruction is composed of a plurality of different fields. The instruction is actually a complex instruction ...separate instructions are sent simultaneously to each execution unit...")

-combining said at least two Single Instruction/Multiple Data operations to execute in a single instruction cycle to thereby yield the compound Single Instruction/Multiple Data instruction.

(Scallon: Col. 4, lines 56-60, "The execution units (ALUs)...are performing parts of a single computational problem in contrast to the MIMD systems...)

Although Scallon failed to explicitly suggest 'selecting' and 'combining' instructions, he did disclose combining instructions to form complex instructions, for the purpose of improving throughput. At col. 4, lines 30-33, Scallon disclosed prior art SIMDs feeding the same instruction to a plurality of ALUs, in contrast to his invention, which sends separate (combined SIMD) instructions.

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Scallon's invention, to more explicitly disclose selecting and combining

instructions, forming complex instructions, as he did similarly suggest combining instructions for the purpose of improving throughput (col. 1, line 63-65), "...to maximize data throughput by making efficient use of the operating capabilities of each of the arithmetic an logic units..."

8. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 4,574,348 to Scallon, in view of US Patent 6,513,146 B1 to Yonezawa et al.

Per claim 2:

-evaluating a processing throughput of the compound Single Instruction/Multiple Data instruction;

(Scallon: Col. 5, lines 43-46, "The parallel connected ALUs may be allocated to different functions thus permitting a problem to be broken down into multiple parallel strings to enable high throughput." Scallon gave consideration to efficient throughput.)

Scallon failed to consider power consumption.

However, Yonezawa disclosed:

-determining a power consumption of the compound Single Instruction/Multiple Data instruction;

(Yonezawa: Abstract, lines 3-8, "...power consumption of each function is estimated through an operation description analysis of functions...so as to determine S/W and H/W implementation. Col. 3, lines 60-61, "...analyzing power consumption...", col. 4, line 5, "...estimating power consumption..." when determining the design of an integrated circuit and partitions software and

hardware (col. 16, lines 16-24).

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention to modify Scallon's invention that uses complex instructions while seeking to provide (col. 1, lines 30-32) "a physically small and light-weight computing device...capable of high throughput..." in contrast to prior art machines that had (col. 1, line 35) "large power requirements...", by combining features as disclosed by Yonezawa to determine the power consumption, because both inventions give consideration to power consumption and throughput (Yonezawa, col. 1, lines 19-20) in the design of efficient integrated circuits.

Per claim 3:

-associating an energy consumption value with at least one micro-operation of the compound Single Instruction/Multiple Data instruction;

(Yonezawa: Col. 2, lines 45-50, "...obtaining power consumption of each function by analyzing functions included in a system operation description language describing operation...")

-minimizing the sum of the energy consumption value.

(Yonezawa: Col. 2, lines 50-54, "...partitioning the function into a H/W implemented function when the power consumption of the function exceeds a threshold value and into a S/W implemented function when the power consumption is smaller than the threshold value...")

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the

invention to modify Scallon's invention that uses complex instructions while seeking to provide (col. 1, lines 30-32) "a physically small and light-weight computing device...capable of high throughput..." in contrast to prior art machines that had (col. 1, line 35) "large power requirements...", by combining features as disclosed by Yonezawa to determine the power consumption, because both inventions give consideration to power consumption and throughput (Yonezawa, col. 1, lines 19-20) in the design of efficient integrated circuits.

9. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 4,574,348 to Scallon, in view of US Patent 6,513,146 B1 to Yonezawa et al., and further in view of "SPONSOR'S FEATURE – DSP PROCESSORS Power and efficiency Architectures for this Century's applications", by Richard Oed and Marcus Gossler (Summer 2001 / Texas Instruments).

Per claims 4-12:

-the compound Single Instruction/Multiple Data instruction includes a vector add-subtract operation / a vector minimum-difference operation / a vector compare-maximum operation / a vector absolute difference and add operation / a vector average operation / a vector scale operation / a vector conditional negate and add operation / a vector select and viterbi shift left operation.

Scallon failed to disclose specific operations of the system. Yonezawa disclosed (col. 3, lines 44-47), "...inputting a system operation description language describing operations of the

semiconductor integrated circuit device to be designed...", but failed to disclose specific operations.

Oed and Gossler disclosed (page 1, paragraph 4) "Two new dsp architectures...satisfy the demand for calculation power...and power efficiency..."
Page 1, paragraph 9, "The improvement in code efficiency is based on the fact that the new processor generation does not used fixed length instructions...they can now use words...New instructions have been added to allow more operations in parallel, ..These parallel instructions are supported by functional units like a second multiply accumulate unit and a second arithmetic logic unit..." Page 2, paragraph 2, "his improvement has been achieved by extending the cpu core – allowing better parallelism – and by adding special image processing instructions...a risc architecture...Algorithms live vector product, Reed-Solomon decoding or motion estimation can be speeded by a factor of seven." Page 2, paragraph 4, "Additionally, the chip has a Viterbi coprocessor..."

Thus, Oed and Gossler disclosed instructions combined into words, newly added instructions, a RISC architecture, and the Viterbi operation. Instructions are added to allow more operations in parallel. Page 1, paragraph 2, "...support has been added to dsps for such features as circular addressing – needed by digital filters – and hardware for loop constructs. This led to several dsp families each specializing in a certain area."

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the

invention to modify Scallon / Yonezawa, by giving consideration to Oed and Gossler who disclosed specialized operation instructions to satisfy the need for calculation power and power efficiency (page 1, paragraph 4), as Scallon disclosed (col. 1, lines 63-65) the need "to maximize data throughput by making efficient use of the operating capabilities of each of the arithmetic and logic units".

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,513,146 B1 to Yonezawa et al., in view of US Patent 4,574,348 to Scallon.

Per claim 15:

-at least one of the micro-operations of the software algorithm is executed on a Single Instruction/Multiple Data processing unit.

Yonezawa failed to disclose SIMD processing unit. However, Scallon disclosed combined SIMD instructions to increase throughput in DSP architecture. Col. 4, lines 43-58, "In FIG. 3, an instruction processing unit generates the sequential instruction stream but each generated instruction is composed of a plurality of different fields. The instruction is actually a complex instruction...The execution units (ALUs) although operating independently, are performing parts of a single computational problem..."

Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Yonezawa's invention to specify that the micro-operation may be executed

on a Single Instruction / Multiple Data processing as suggested by Scallon, because both inventions are directed to increasing throughput while reducing power consumption in the design of a DSP instruction set.

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent 6,513,146 B1 to Yonezawa et al.

Per claim 16:

A method for estimating the absolute power consumption of a software algorithm, comprising:

-determining a plurality of relative power estimates of instructions of a microprocessor;

(Yonezawa: Col. 2, lines 47-50, "...obtaining power consumption of each function by analyzing functions included in a system operation...". Col. 2, lines 56-57, "...estimating the power consumption of each function...")

-simulating a software algorithm including one or more compound instructions;

(Yonezawa: Col. 4, lines 36-37, "...power analyzing means for conducting simulation (simulating)...in accordance with the source program (software algorithm)...")

-determining an absolute power estimate of a software algorithm to be executed by the microprocessor based on the relative power estimates.

(See rejection of limitations as addressed in claims 13 and 14 above.)

Yonezawa failed to explicitly disclose "absolute power consumption", bud did disclose (col. 4, lines 34-40) "power information storing means for storing power information...and power analyzing means for conducting simulation...and analyzing power consumed in executing the source program...", which broadly may infer "estimating the absolute power consumption". Therefore, it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to modify Yonezawa's invention to include "absolute power consumption."

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Also note:

US Patent 5,649,179 to Steenstra et al.

Steenstra disclosed a method for programming and controlling SIMD processors by dynamically allocating instructions. "The first step...it to parse...instruction targeted for the SIMD processor into components that effect the operation of a given processing element...In step 2, the components are assembled into a control specification for the processing element decoder (col. 2, lines 24-28)". Col. 1, lines 19-22, "The disadvantage of wide instruction words...increases power consumption..." Col. 5, lines 41-51, "The dynamic allocation of instructions to processing elements in a SIMD processor is advantageous...the SIMD processor instruction word length can be minimized..."

US Patent 5,818,788 to Kimura et al.

Kimura disclosed, using a SIMD architecture, "the order of issued addresses can change, be shifted, in order to minimize the number of word addresses changed, and the order can be restored to the original sequence after a memory access...(col. 6, lines 5-9)." "With the above mentioned arrangement, a high-speed, low-power and highly-stable logic integrated...SIMD architecture can be realized (col. 6, lines 9-11)." Kimura alters accesses to registers or memory blocks using the clock with a timing skew to reduce the peak current flow (col. 6, lines 50-65).

US Patent 6,151,568 to Allen et al.

Allen disclosed an invention that analyzes and calculates power consumed (col. 2, lines 28-29), generates power consumption estimation (col. 2, line 53), using a simulator (col. 2, line 56), and writes to a scenario database (col. 5, line 50).

US Patent 6,513,145 to Venkitakrishnan.

Venkitakrishnan disclosed a method for estimating the maximum power consumed, estimating power consumption by modeling a benchmark, summarizing the results (Abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan

Q. Dam can be reached at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman

01/03/2005

WEI Y. ZHEN
PRIMARY EXAMINER